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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
MOLL, JESSE R	
ART UNIT	PAPER NUMBER
2181	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/09/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/757,939	HANSEN ET AL.	
	Examiner	Art Unit	
	Jesse R. Moll	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *24 October 2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-24 have been examined.

Withdrawn Rejections

2. Applicant, via amendment, has overcome the rejection of claims 5 and 17 under 35 U.S.C. 112 second paragraph. The rejection has been respectfully withdrawn.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Ito et al. (U.S. Patent No. 5,742,782), herein referred to as Ito et al.'782.

5. Referring to claim 1, Ito et al.'782 discloses, as claimed, a programmable processor (see Fig. 1) comprising: a data path (comprising execution parts 25a-25d, see Fig. 1); an external interface operable to receive data from an external source (certainly existing in Ito et al.'782's system for handling input/output operation for peripherals) and communicate the received data over the data path; a register file containing a plurality of registers (register parts 26a-26c, see Fig. 1) each having a register width (including at least 173 and 174, se Fig. 6), the register file coupled to the data path and operable to support processing of a plurality of threads (Threads A, B, and C, see Fig. 3); an execution unit (execution parts 25a-25d, see Fig. 1) coupled to the data path, the execution unit operable to execute a plurality of instruction streams from the plurality of threads (Threads A, B, and C, see Figs. 3 and Fig. 15A), each instruction stream including a single instruction that operates on a plurality of data elements (data area 173, see Fig. 6) in partitioned fields of at least one of the registers (register parts 26a-26c, see Fig. 1) to produce a catenated result, each of the data elements (data area 173, see Fig. 6) having an elemental width smaller than the register width (including at least 173 and 174, se Fig. 6). Note claims 8, 13, and 20 recite the corresponding limitations as set forth above in claim 1. Ito et al.'782 also discloses as to Claims 8 and 20 first and second registers (register parts 26a-26c, see Fig. 1).

6. As to claim 2, Ito et al.'782 also discloses: the processor of claim 1 wherein the execution unit (execution parts 25a-25d, see Fig. 1) comprises a pipeline (see Fig. 15B) having a plurality of stages and wherein the pipeline interleaves execution of instructions (such as A1-A12, B1-B10, and C1-C10, see Fig. 15A) from the plurality of instruction streams. Claims 9, 14, and 21, recite the corresponding limitations as set forth above in claim 2.

7. As to claim 3, Ito et al.'782 also discloses: the processor of claim 2 wherein the pipeline is operable to simultaneously contain states of execution of at least two instructions (such as A1-A12, B1-B10, and C1-C10, see Fig. 15A) from different instruction streams. Claims 10, 15, and 22 recite the corresponding limitations as set forth above in claim 3.

8. As to claim 4, Ito et al.'782 also discloses: the processor of claim 2 wherein execution of the instructions (such as A1-A12, B1-B10, and C1-C10, see Fig. 15A) is interleaved in a round-robin manner (see Fig. 15B). Claims 11, 16, and 23 recites the corresponding limitations as set forth above in claim 4.

9. As to claim 5, Ito et al.'782 also discloses: the processor of claim 1 wherein the processor ensures only one thread from the plurality of threads (Threads A, B, and C, see Figs. 3 and Fig. 15A) can handle an exception at any given time (see Col. 12, lines 17-23, regarding handling the exception in the Ito et al.'782's system and note one

decoder (23a-23c) is handling one threat only see Fig. 1). Claim 17 recites the corresponding limitations as set forth above in claim 5.

10. As to claim 6, Ito et al.'782 also discloses: the processor of claim 1 further comprising a virtual memory addressing unit and a cache operable to store data communicated between the external interface (certainly existing in Ito et al.'782's system for handling input/output operation for peripherals) and the data path. Claim 18 recites the corresponding limitations as set forth above in claim 6.

11. As to claim 7, Ito et al.'782 also discloses: the processor of claim 1 wherein the execution unit is further operable to, in response to decoding a second single instruction specifying a first and a second register (register parts 26a-26c, see Fig. 1) each containing a plurality of operands (such as source1 167 and source 2 and destination register No. 166, see Fig. 9 (a)-(c)), multiply (such as Fmult operation, see Col. 4, lines 31) the plurality of floating point operands (Fmult operation, see Col. 4, lines 31, using floating point operands) in the first register by the plurality of operands (such as source1 167 and source 2 and destination register No. 166, see Fig. 9 (a)-(c)) in the second register to produce a plurality of products and provide the plurality of products to partitioned fields of a result register (register parts 26a-26c, see Fig. 1) as a second catenated result. Note Claims 12, 19, and 24 recite the corresponding limitations as set forth above in claim 7.

Response to Arguments

12. Applicant's arguments filed 24 October 2006 have been fully considered but they are not persuasive.

13. Applicant states:

> Applicants respectfully submit that Ito fails to anticipate claim 1. Claim 1 relates to a SINGLE instruction specifying an operation that is to be performed on each one of a plurality of data elements in partitioned fields of at least one register. By contrast, Ito discloses a traditional technique for MULTIPLE instructions to operate on data stored in separate registers. It is believed that even without the current amendment, claim 1 clearly distinguishes from the multiple-instructions technique of Ito. However, in the interest of expediting prosecution of the present application, claim 1 has been amended to further highlight the significant difference between the present invention and Ito.

Examiner disagrees. The instruction bits for all three threads are considered to be a single instruction. An instruction is merely a grouping of bits which force a processor to operate in a certain manner. For example, a VLIW instruction contains multiple parts, but is still considered to be a single instruction.

14. Applicant states:

> Ito fails to disclose such a single instruction that specifies an operation that is to be performed on each one of a plurality of data elements in partitioned fields of at least one register. Ito describes a traditional technique requiring multiple instructions that specify different operations to be performed on data in separate registers. Fig. 8 of Ito, which is cited by the Examiner and is reproduced below, clearly illustrates Ito's multiple instructions: As seen in this figure, Ito discloses multiple instructions, namely 4 instructions: (1) an "L/S" instruction, (2) an "FAdd" instruction, (3) an "FMult" instruction and (4) a "FixOp" instruction. These 4 instructions specify 4 different operations that are performed on data stored in separate registers. The "L/S" instruction specifies a load/store operation performed on data in a first set of registers. The "FAdd" instruction specifies a floating-point add operation performed on data in a second set of registers. The "FMult" instruction specifies a floating-point multiply operation performed on data in a third set of registers. The "FixOp" instruction specifies an integer operation performed on data in a fourth set of registers. See Ito, col. 4, lines 9-22. The four sets of registers are specified by four sets of "source 1 register number holding latches" (175) and "source 2 register number holding latches" (176) shown in Fig. 6 of Ito. See Ito, col. 13, lines 33-49.

> Thus, Ito's 4 instructions specify 4 completely different operations to be performed on data in different registers. In fact, Ito employs 4 different execution devices that independently perform these 4 different operations so as to not interfere with one another. See Ito, col. 6, lines 27-29 ("An the respective instruction execution parts 25 are operated independently without interference with each other").

Examiner disagrees. All four instructions are considered to perform a single operations for the same reasons as discussed above.

15. Applicant states:

> Furthermore, Ito also fails to disclose an operation that is performed on each one of a plurality of data elements to produce a catenated result, as recited in claim 1. As mentioned previously, Ito discloses 4 instructions that specify 4 completely different operations to be performed on data in separate registers. These 4 different operations independently generate 4 individual results that are never catenated together. Instead, the 4 individual results are written to 4 separate destination registers. The 4 destination registers are specified by four sets of "destination register number holding latches" (177) shown in Fig. 6 oflto. See Ito, col. 13, lines 50-55. By writing the 4 individual results to separate registers, Ito not only fails to disclose, but in fact teaches away from, the production of a catenated result. For this additional reason as well, Ito fails to anticipate claim 1.

Examiner disagrees. All four instructions are considered to perform a single operations for the same reasons as discussed above.

16. With respect to the arguments regarding claim 6, Examiner disagrees. Any communication with an external device (with an external memory space) can be considered to be virtual memory addressing. Further, accessing main memory can be considered using virtual memory (with respect to the internal registers). The limitation "virtual memory addressing" is extremely broad.

17. With respect to the arguments regarding claim 7, Examiner disagrees. The limitation "register" merely requires a storage location to store a plurality of bits. Any number of storage locations can be considered as a single register. One example of this would be a register to hold multiple flags. Clearly, a group of flags can be considered as one register. In the same way, multiple storage locations (for operands) can be considered to be a single register. The limitation of these two storage locations being 1 register imposes no physical limitations on the invention.

18. For at least the reasons stated above, Examiner respectfully disagrees with the alleged patentability of claims 1-24.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse R. Moll whose telephone number is (571)272-2703. The examiner can normally be reached on M-F 10:00 am - 6:30 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald A. Sparks can be reached on (571)272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jesse R Moll
Examiner
Art Unit 2181

JM 2/5/07

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SUPERVISORY PATENT EXAMINER